FACTSHEET RA12 version 1.0

13.56-MHz Multi-Standard RFID Reader IC

Features Summary

Hi light Features

- Low Power Card Detection
- External RF Field Detection
- Support Protocol
  - ISO14443A/B, all bit rates
    - 106, 212, 424 and 848 kbps
  - ISO15693, all modes
    - Downlink 1 of 4 and 1 of 256
    - Uplink 6.6 / 26 kbps with 1 & 2 sub-carrier
  - NFC Tag Type 1 & PicoTag
  - NFC Bar Code Data Format

Transmitter

- Proximity operating distance up to 10 cm (based on 3x4 cm^2 antenna)
- Modulation index adjustable by software
- Transmission supply current up to 250mA at 5.0V T_VDD
- Driver Output Impedance 3 Ohms at 5V T_VDD
- Arbitrary modulation by external signal
- Wide operating voltage for Tx from 2.7V to 5.5 V
- On-chip Framing coder for supported standards

Receiver

- Rx sensitivity down to 2 mVp
- On-chip Framing decoder for supported standards
- Automatic Gain Control (AGC)

Interface & Peripheral

- 4-wires SPI Interface up to 10 Mbps
- 64-byte send and receive data FIFO-buffer
- Interrupt (IRQ) PIN
- Programmable timer
- Low jitter on-chip oscillator buffer
- Ultra-low quiescent current On-Chip 150 mA 3.3V LDO regulator for external microcontroller

Operating Conditions

- Operating temperature : -40 to 85 °C
- Operating voltage :
  - Receiver A_VDD : 2.7 to 3.6 V
  - Transmitter T_VDD : 2.7 to 5.5 V
  - Digital I/O IO_VDD : 2.7 to 5.5 V
- Power Saving Mode
  - Hard Power Down : 0.5 uA
  - Soft Power Down : 4.7 uA
  - Standby : 1.0 mA
  - Card Detection – sleep : 4.7 uA

Applications

- Secure Access Control / Door Lock
- Toy
- Handheld RFID Reader
- Contactless payment system

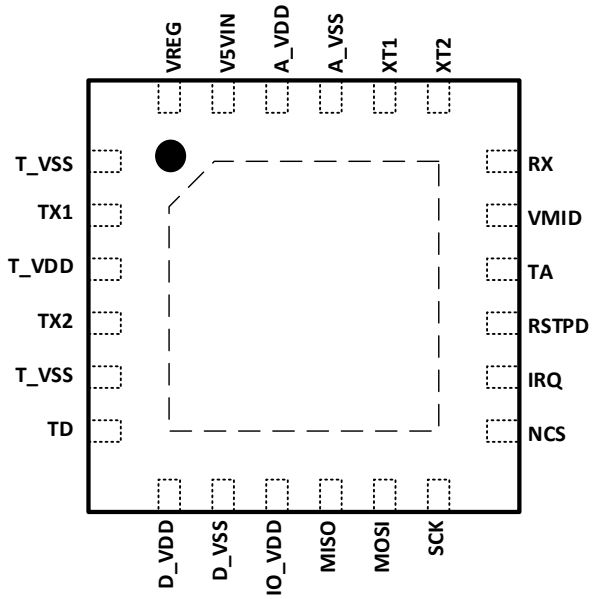
Package

- Small QFN4x4 24-Pin with Heat sink pad
- Tested sawn wafer

Ordering Information

Part No.	Description	Marking
P002HRA12QFN4-01	RA12, 13.56Hz RFID Reader IC, ISO14443A/B and ISO15693 protocols, QFN 4x4 Package, IC	0ABXY
TBA	RA12, 13.56Hz RFID Reader IC, ISO14443A/B and ISO15693 protocols, DOW	TBA

1.General Description



Die and Pad location

The RA12 is a single-chip reader ASIC for 13.56-MHz RFID/contactless standard protocols. The RA12 supports and compatibles with all major global secured baseband ISO standards including ISO14443 Type A, Type B, Crypto_M cards, and Smartlabel ISO15693. The RA12 provides a hi-speed SPI controller/host interface with a built-in 64-byte FIFO for smooth data transfer. Furthermore, the embedded codec is capable of handling all bit-level coding/encoding, encrypting/decrypting as well as frame-level manipulation for transmission and reception. The chip is well suited for mobile devices due to its low power consumption and low operating voltage from 2.7-3.6 V. The ultra low power on-chip 3.3V regulators are provided to stabilize the chip's power, and simultaneously supply the power to the external companion microcontroller up to 150 mA.

The RA12 receiver circuit incorporates a full AGC loop allowing a wide dynamic range of RF input signal levels. The chip's excellent sensitivity performance enables detection of the input signals with amplitudes as low as 1mVpkpk without distorting the data integrity. The receiver filters can be selected optionally either to a predefined band in accordance with the generic required standard setup, or to an arbitrarily defined combination which gives flexibility to cope with various antenna variations/parameters. The baseband circuits permit the inbound/outbound configuration to accept various forms of customized protocols, incoming to the chip and outgoing to the external RF circuitry in the application specific-design system.

The transmitter is capable of accepting a wide range of operating supply voltages to serve various applications, e.g., 5V for base stations or desktop readers, and 3.3V for handheld devices. The transmission controller is entirely used to support all operation status and requests, including FIFO status full/high/low and Transmission complete flag. The transmitter drivers support a wide range of power supply voltages from 2.7 to 5.5 V. A high drive current up to 250 mA is guaranteed for demanding item-level mid-range reader designs. The dual high-powered transmitters can be flexibly configured in various configurations, e.g. differential driving, single-ended driving, and a mode to drive an external Class-E amplifier for improving the drive strength in the gate antenna setup.

The ultra-low power on-chip 3.3V regulator provides stable supply voltage to external companion microcontroller with capability up to 150 mA.

The RA12 contains efficient power saving modes: hard power down, soft power down, standby and low-power card detection. The low-power card detection mode allows the chip to not operate at full power continuously. The chip periodically senses the external card. if external card is detected, interrupt signal will be sent to MCU to wake up the system.

To facilitate operation of the companion microcontroller, the RA12 is fully equipped with on-chip peripheral support devices such as an RF-trig timer; a host interrupt generator, and a clock divider. The RA12 is offered in a QFN package with excellent heat dissipation when self-mounted on PCB.

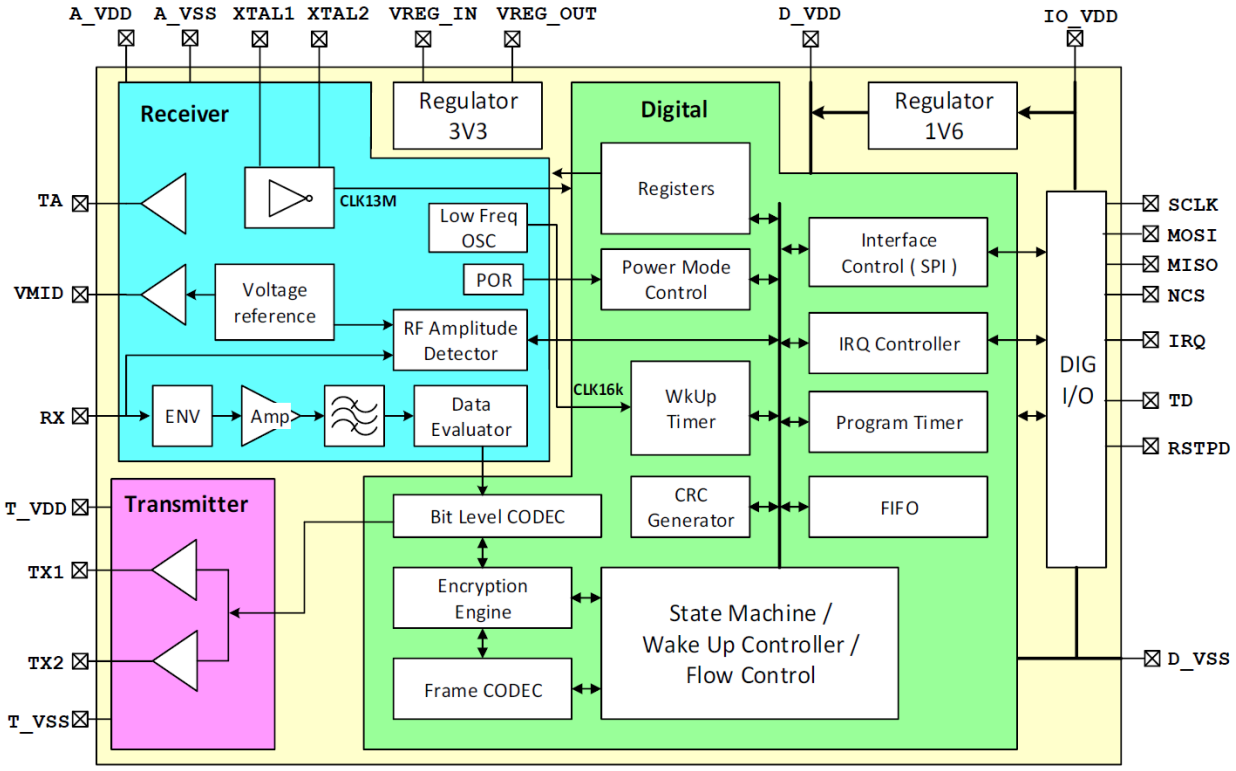


Figure 1-1: Functional block diagram

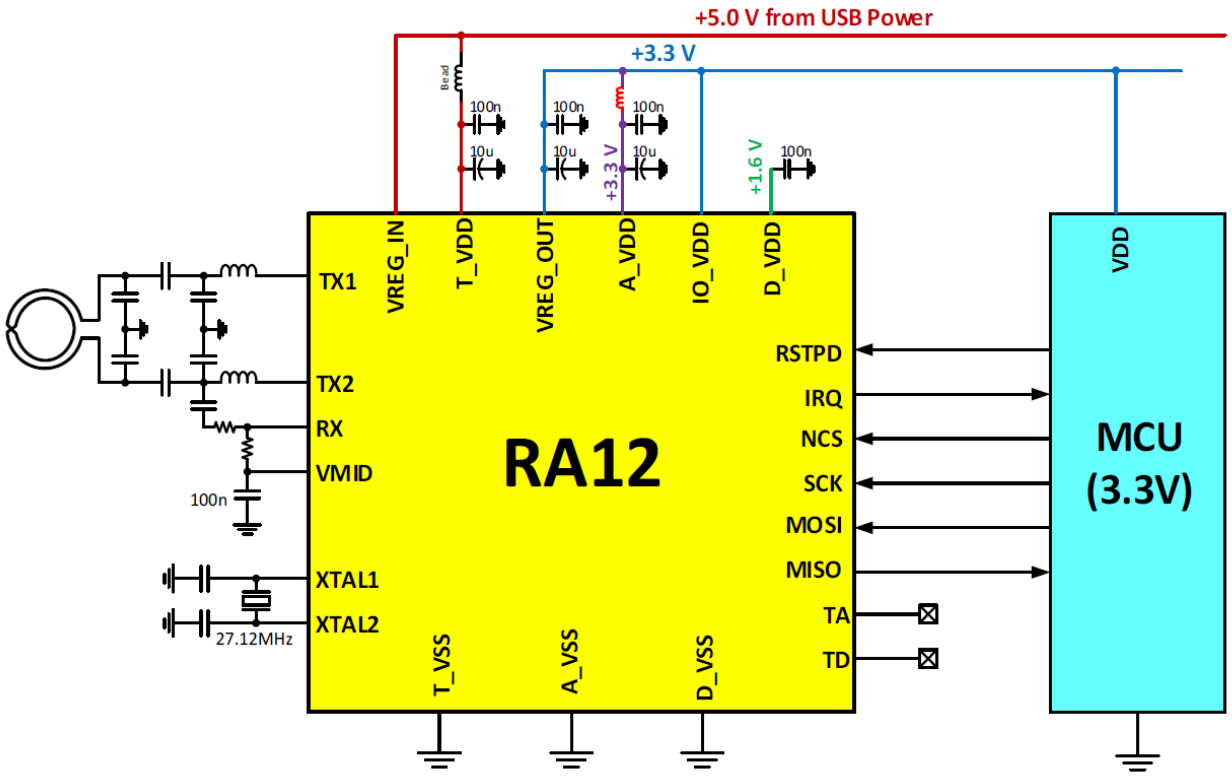


Figure 1-2 Typical configuration employing on-chip regulator for MCU with 3.3V I/O

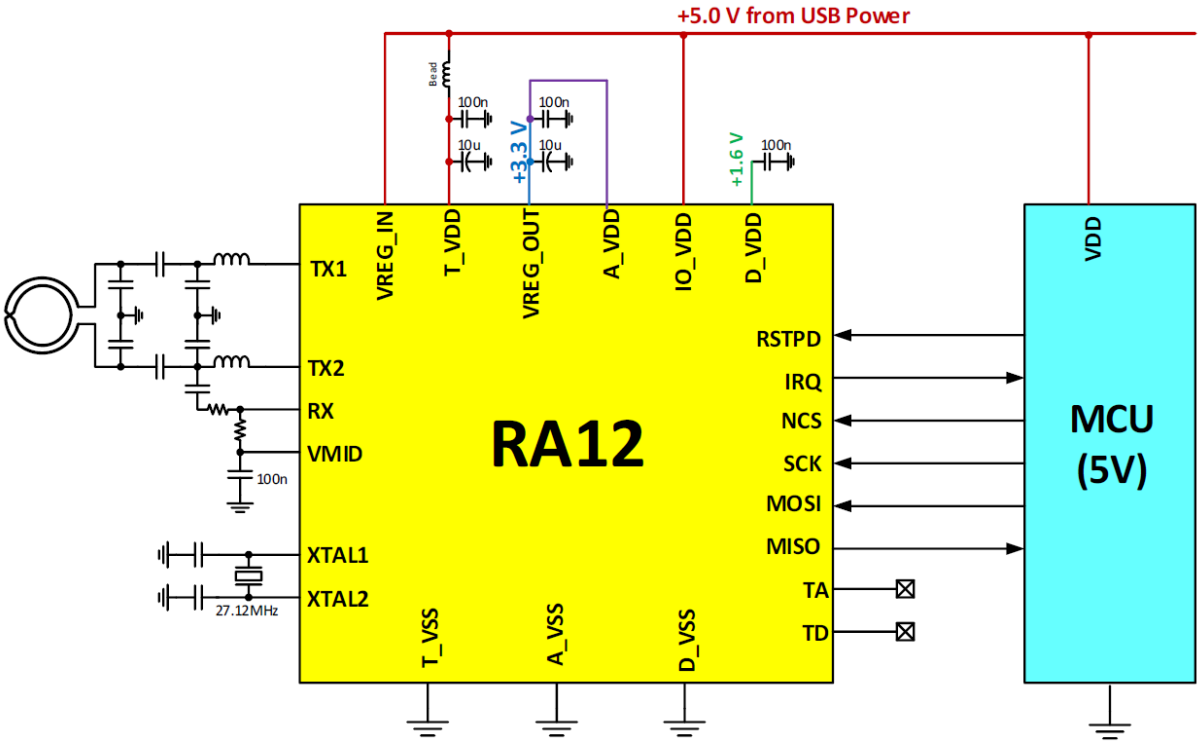


Figure 1-3 Typical configuration employing on-chip regulator for MCU with 5V I/O

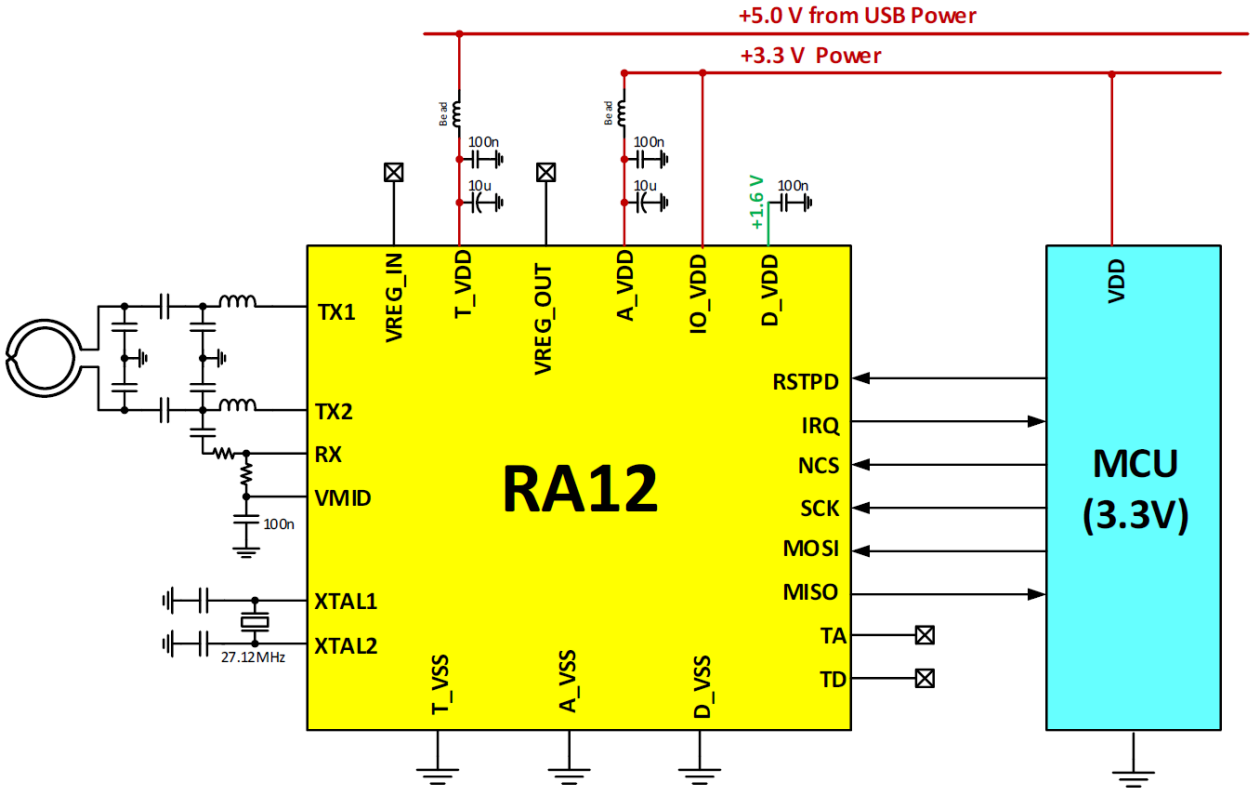


Figure 1-4 Typical operating circuit for external power supply (not apply 3.3V on-chip regulator)

2. Pin Information

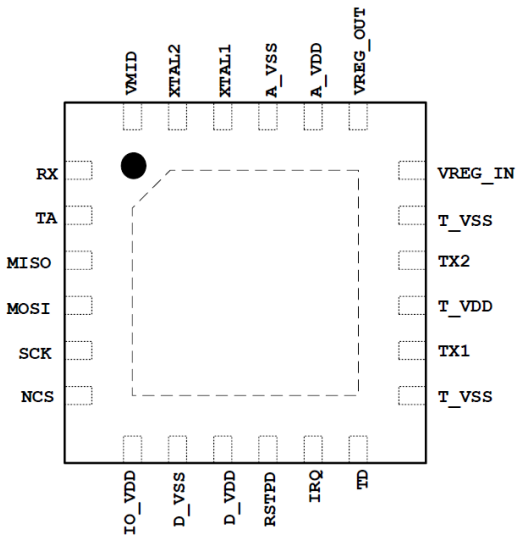


Figure 2-1: Pin Package Information (Top View)

Table 2-1: Pin description

Pin	Symbol	Type	Description
1	RX	Analog Input	Receiver input
2	TA	Analog Output	Analog Test Pin
3	MISO	Digital Input	SPI : Master In Slave Out
4	MOSI	Digital Output	SPI : Master Out Slave In
5	SCK	Digital Input	SPI : Clock input
6	NCS	Digital Input	SPI : Chip Select (Active Low)
7	IO_VDD	Power	Digital I/O Power supply
8	D_VSS	Power	Digital and Digital I/O Ground
9	D_VDD	Power	Digital Core Power Supply (need external decoupling capacitor 100 nF)
10	RSTPD	Digital Input	Master Reset (Active High)
11	IRQ	Digital Output	Interrupt Request
12	TD	Digital I/O	Digital Test Pin
13	T_VSS	Power	Transmitter Ground
14	TX1	Out	Transmitter Output # 1
15	T_VDD	Power	Transmitter Power Supply
16	TX2	Out	Transmitter Output # 2
17	T_VSS	Power	Transmitter Ground
18	VREG_IN	Power	On-Chip Regulator input (5.0 V)
19	VREG_OUT	Power	On-Chip Regulator output (3.3 V)
20	A_VDD	Power / Regulator output	Analog Power Supply / On-Chip Regulator Output (3.3 V) (need external decoupling capacitor 100 nF when use on-chip regulator)
21	A_VSS	Power	Analog Ground
22	XTAL1	Analog Input	Crystal oscillator input
23	XTAL2	Analog output	Crystal oscillator output
24	VMID	Analog Output	Mid Rail Reference Voltage

3. Electrical specification

Table 3-1 Operating condition

Parameter	Description	Min	Typ	Max	Unit	Conditions
A_VDD	Analog Power Supply Voltage	2.7	3.3	3.6	V	
IO_VDD	Digital Input Output Power Supply	2.7	3.3	5.5	V	
D_VDD	Digital Power Supply Voltage	1.54	1.65	2.2	V	Regulated from internal
T_VDD	Transmitter Power Supply Voltage	2.7	5	5.5	V	
ESD	Electrostatic discharge tolerance		1.5		kV	HBM model
VPOR	Reset Trigger voltage	2.3	2.4	2.6	V	IO_VDD & A_VDD

Table 3-2: Power consumption

Parameter	Description	Min	Typ	Max	Unit	Conditions
I_A_VDD	Analog Power Supply Current A_VDD = 3.3V		5.5	6.4	mA	Active state (receiver on)
			0.8	1.0	mA	Idle state (receiver off)
				0.2	uA	Hard Power down, (Pin **RSTPD** = 1)
			1.7	2.4	uA	Soft Power down (**Powerdown** bit = '1'), 25°C
				3.5	uA	Soft Power down (**Powerdown** bit = '1'), -40°C to 85 °C
			0.7	0.9	mA	Standby (**Standby** bit = '1')
			1.7	2.4	uA	WakeUp Card Detection Mode (**WkUpCD** bit = '1') – ***"Sleep"*** (1) , 25°C
			3.0	3.3	mA	WakeUp Card Detection Mode (**WkUpCD** bit = '1') – ***"Detect"*** (1)
I_IO_VDD	Digital I/O Power Supply Current (also include digital core current) IO_VDD = 3.3V		1.0	1.2	mA	Active State (CODEC On)
			0.9	1.1	mA	Idle state (CODEC off)
				0.2	uA	Hard Power down, (Pin **RSTPD** = 1)
			3.0	4.2	uA	Soft Power down (**Powerdown** bit = '1'), 25°C
				7.0	uA	Soft Power down (**Powerdown** bit = '1'), -40°C to 85 °C
			0.3	0.5	mA	Standby (**Standby** bit = '1')
			3.0	4.2	uA	WakeUp Card Detection Mode (**WkUpCD** bit = '1') – ***"Sleep"*** (1) , 25°C
			0.9	1.1	mA	WakeUp Card Detection Mode (**WkUpCD** bit = '1') – ***"Detect"*** (1)
Itotal	Total power supply current I_IO_VDD + I_A_VDD + I_T_VDD **IO_VDD = A_VDD = T_VDD** = 3.3 V , I_TX = 100 mA Not apply on-chip 3.3V regulator, VREG_IN and VREG_OUT are not connected		6.6	7.6	mA	Active state (receiver on, transmitter off)
			1.7	2.1	mA	Idle state (receiver off, transmitter off)
				0.8	uA	Hard Power down, (Pin **RSTPD** = 1)
				11.0	uA	Soft Power down (**Powerdown** bit = '1'), 25°C
			1.0	1.4	mA	Standby (**Standby** bit = '1')
			10.4		uA	Average at WakeUp Card Detection Mode at Twkup = 500 ms, transmitter on periodically (calculated)
			7.5		uA	Average at WakeUp Card Detection Mode at Twkup = 1000 ms, transmitter on periodically (calculated)

(1) : Average power in Card Detection Mode depends on duty cycle between *Sleep* and *Detect* period.

Table 3-3: Transmitter characteristic

Parameter	Description	Min	Typ	Max	Unit	Conditions
I_TX	Transmitter current, continuous wave			250	mA	T_VDD = 5V, 25 °C, Average current
Z_Tx, min	Minimum equivalent Tx Output impedance (**GsCfgCW** = 0x3F)		3	5	Ohm	T_VDD = 5V, 25 °C
I_T_VDD, static	Transmitter Static Power supply Current		7		mA	Pin **Tx1** & **Tx2** are unconnected **RF1En** = 1, **RF2En** = 1 T_VDD = 5 V
M	Adjustable Modulation index	0		60	%	T_VDD = 5V, **100ASK** = 0
				100	%	T_VDD = 5V, **100ASK** = 1

Table 3-4: Receiver characteristics

Parameter	Description	Min	Typ	Max	Unit	Conditions
VSEN	Receiver input sensitivity		2.0		mVp	A_VDD = 3.3V
PSRR	Power supply rejection ratio		40		dB	A_VDD = 3.3V + 0.2*sin(1MHz)
VRx	Rx input voltage range	0.0		3.3	V	A_VDD = 3.3 Volt, **BypassENV** = '0'
		0.5		2.8		A_VDD = 3.3 Volt, **BypassENV** = '1'
VCar,Min	Minimum Carrier for envelope detector		0.25		Vp	
VVMID	VMID Voltage	1.63	1.65	1.67	V	A_VDD = 3.3 V
ZVMID	VMID output impedance @ 13.56 MHz			0.5	ohm	CL = 100nF, A_VDD = 3.3 V
Gain	Gain (Measured from Rx input to the output of the internal last amplifier)			48	dB	**Gain** = 11b, **Gain_ST3** = 000b
		12			dB	**Gain** = 00b, **Gain_ST3** = 000b
Gstep	Gain step		3		dB	**AGC_EN** = 1
			12		dB	**AGC_EN** = 0 Defined by Gain [1:0]
Rxnoise	Intrinsic input referred noise in Rx		TBA			
FD,Min	Minimum RF amplitude @ **RX** pin for external RF field detection.		10		mVp	RF input at RX pin is in phase with internal clock. When the phase is different this value will be more.
CD,Min	Minimum RF amplitude changing @ **RX** pin for Card detection.		10		mVp	

Table 3-5: On Chip Regulator

Parameter	Description	Min	Typ	Max	Unit	Conditions
VREG_IN	Regulator input voltage	3.6	5	5.5	V	
VREG_OUT	Regulator output voltage	3.25	3.3	3.35	V	Iout = 10mA, 25 °C
IOUT	Output regulator current			150	mA	
$\Delta Vout_{LineReg}$	Line regulation (ΔVout)		0.5	1	mV/V	Iout = 0 mA , 3.6V < VREG_IN < 5.5V
$\Delta Vout_{LoadReg}$	Load regulation (ΔVout)		0.25		mV/mA	VREG_IN = 5 V , 0 < Iout < 150 mA
IREGq	Regulator Quiescent current		2		uA	No Load, VREG_IN = 5 V , 25 °C
			100		uA	Iout = 100mA, VREG_in = 5V , 25 °C