RA10

13.56 MHz ISO14443A RFID Reader IC

REV 1.0

Features Summary

Support Protocol

- ISO14443 Type-A all bit rates
  - 106, 212, 424 and 848 kbps
- Compatible to Crypto_M

Transmitter

- Proximity operating distance up to 10 cm (based on 3x4 cm2 antenna)
- Maximum driving current up to
- 200 mA/ PIN @ 5V VDDT
- 300 mA/ PIN @ 7V VDDT
- Accept external baseband signal for RF modulation
- Accept wide operating voltage for Tx from 2.7 - 7 V
- On-chip Framing coder

Receiver

- Rx sensitivity down to 1 mVpkpk
- Rx automatic gain control (AGC)
- Accept external baseband signal from external circuitry for frame level processing
- On-chip Framing handler for supported standards

Interface and peripheral

- SPI Interface up to 10 Mbps
- 64-byte send and receive FIFO-buffer
- 64-byte addressing user-configurable registers
- Interrupt (IRQ) PIN
- Programmable timer
- Programmable clock divider for external MCU
- Low jitter on-chip oscillator buffer
- On-Chip Dual 80 mA 3.3V

Operating conditions

- Operating temperature from -40 to 85oC
- Operating voltage from 2.7 to 3.3 V for Receiver
- Operating voltage from 2.7 to 7 V for Transmitter
- 5.5 uA in power down mode
- 1.3 mA in standby mode
- 8.0 mA when all receiver blocks are active
- Small QFN5x5 32-Pin with Heat sink pad or TSSOP-28

Reference Design/ Evaluation Kit

- Ready- to-use USB Module and Generic module
- Demonstration Software/ Sample firmware available

Applications

- Contactless payment system
- Secure access control
- PC peripherals device
- Handheld RFID reader

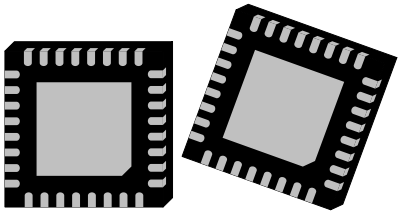
Revision History

Revision	Date	Description	Change / Update / Comment
1.0	25 Feb 2022	1st Release	Official release

Ordering information

Part No.	Description	Package	Marking	Part Status
PI3AVQO7P20UT1001E1	RA10-01, 13.56MHz RFID Reader IC Front-End ISO14443A/NFCtag type 1/2/4A (1st Gen.) QFN 0.85 mm, TnR, IC	32-PIN QFN 5x5 mm	7CAYM	-40°C to +85°C
PI3ATSM6T10UT1001Y1	RA10-01, 13.56MHz RFID Reader IC Front-End ISO14443A/NFCtag type 1/2/4A (1st Gen.) TSSOP, Tube, IC	28-PIN TSSOP	5CAYM	-40°C to +85°C

General Description



32-Pin QFN5x5 Package

The RA10 HiRead-R is a single-chip reader ASIC for 13.56-MHz RFID/contactless ISO14443 Type-A standard protocols, including Crypto_M. The HiRead-R provides a hi-speed SPI controller/host interface with a built-in 64-byte FIFO for smooth data transfer. Furthermore, the embedded codec is capable of handling all bit-level coding/encoding, encrypting/decrypting as well as frame-level manipulation for transmission and reception. The chip is well suited for mobile devices due to its low power consumption and low operating voltage from 2.7-3.3 V. The on-chip 3.3V regulators are provided to stabilize the chip's power, and simultaneously supply the power to the external companion microcontroller up to 80 mA.

The HiRead-R receiver circuit incorporates a full AGC loop allowing a wide dynamic range of RF input signal levels. The chip's excellent sensitivity performance enables detection of the input signals with amplitudes as low as 1mVpkpk without distorting the data integrity. The receiver filters can be selected optionally either to a predefined band in accordance with the generic required standard setup, or to an arbitrarily defined combination which gives flexibility to cope with various antenna variations/parameters. The baseband circuits permit the inbound/outbound configuration to accept various forms of customized protocols, incoming to the chip and outgoing to the external RF circuitry in the application specific-design system. The HiRead-R transmitter is capable of accepting a wide range of operating supply voltages to serve various applications, e.g., base stations, desktop readers, and handheld devices. The transmission controller is entirely used to support all operation status and requests, including FIFO status full/high/low and Transmission/Reception complete. The transmitter drivers support a wide range of power supply voltages from 2.7 to 7 V. A high drive current up to 200 mA is guaranteed for demanding item-level mid-range reader designs. The dual high-powered transmitters can be flexibly configured in various configurations, e.g. differential driving, single-ended driving, and a mode to drive an external Class-E amplifier for improving the drive strength in the gate antenna setup.

To facilitate operation of the companion microcontroller, the HiRead-R is fully equipped with on-chip peripheral support devices such as a voltage reference, an RF-trig timer, a host interrupt generator, and a clock divider. The RA10 is offered in a low-profile QFN package with excellent heat dissipation when self-mounted on PCB.

Block diagram and typical configuration

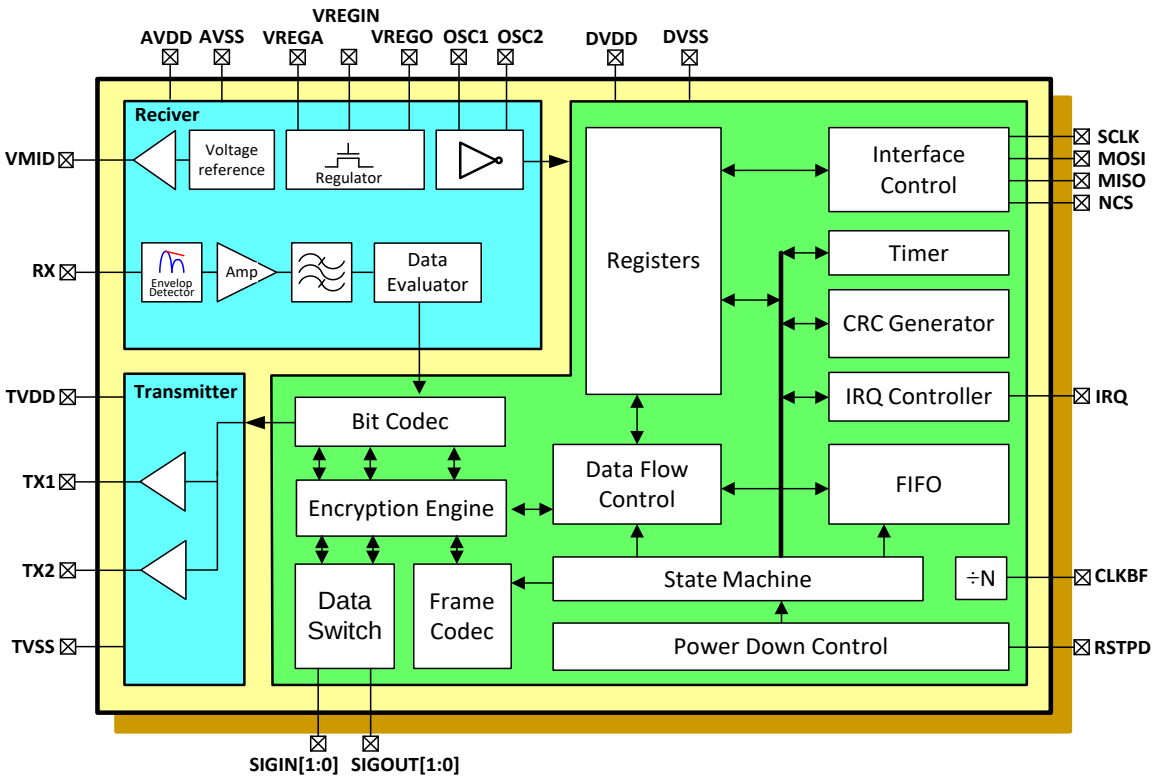


Figure 1 Functional block diagram

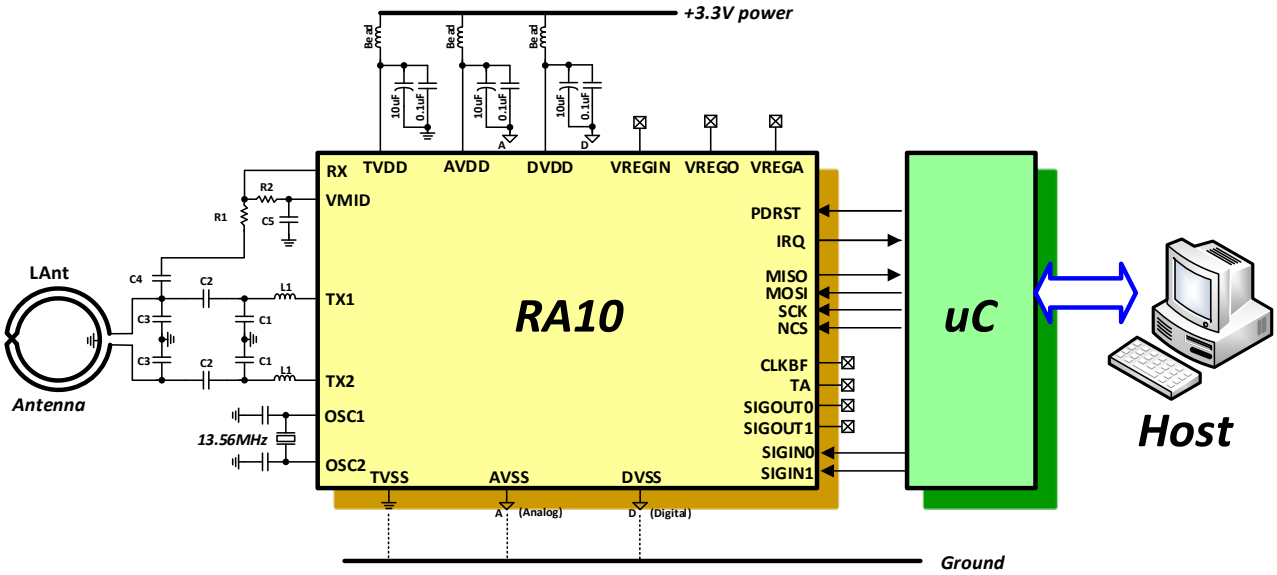


Figure 2 Typical operating circuit

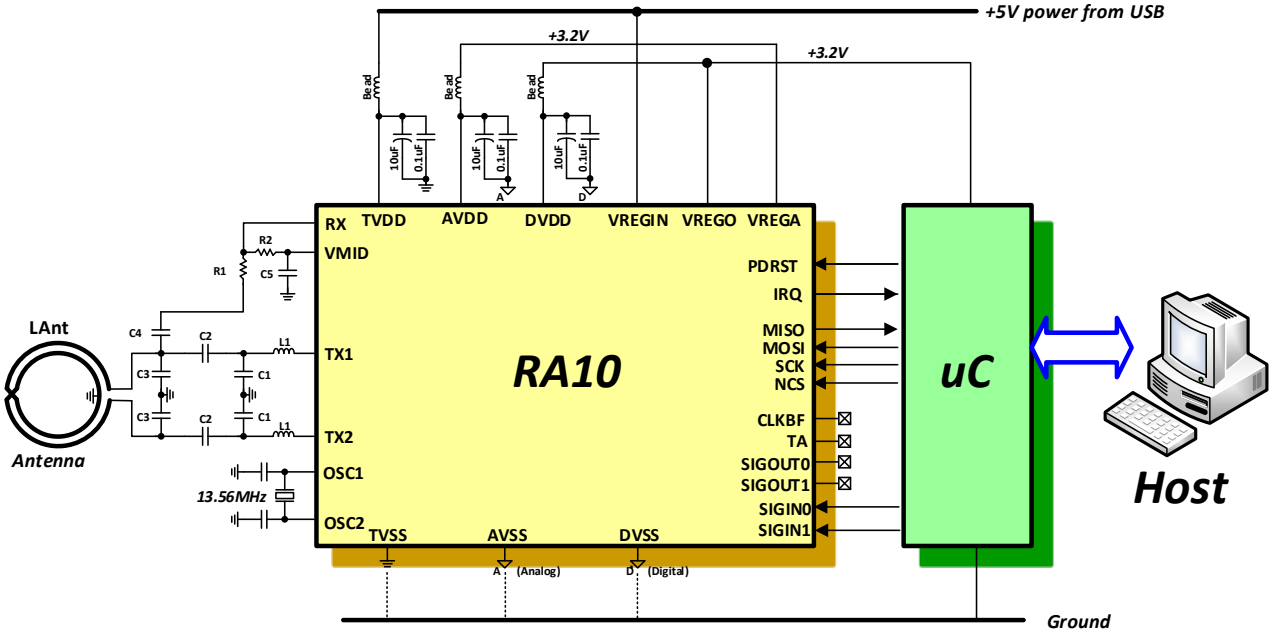


Figure 3 Typical configuration employing on-chip regulator

Pin configuration

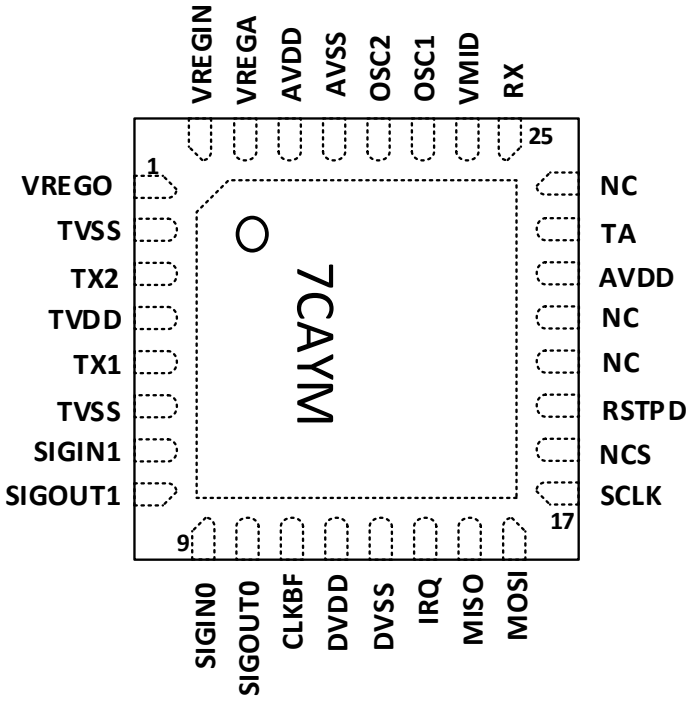


Figure 4 Pin arrangement (top view)

Y : Year Code
M : Month Code

Table 1 Pin Description

Pin	Symbol	Type	Related SUPPLY	Description
1	VREGO	Power	DVDD, DVSS	3.3V Regulator Output for Digital part
2	TVSS	Power	TVDD, TVSS	Transmitter Ground
3	TX2	OUT	TVDD, TVSS	Transmitter Output 2
4	TVDD	Power	TVDD, TVSS	Transmitter VDD
5	TX1	OUT	TVDD, TVSS	Transmitter Output 1
6	TVSS	Power	TVDD, TVSS	Transmitter Ground
7	SIGIN1	IN	DVDD, DVSS	Digital input signal for test mode. If this Pin is unused, tide gnd.
8	SIGOUT1	OUT	DVDD, DVSS	Digital output signal for test mode
9	SININ0	IN	DVDD, DVSS	Digital input signal for test mode. If this Pin is unused, tide gnd.
10	SINOUT0	OUT	DVDD, DVSS	Digital output signal for test mode
11	CLKBF	OUT	DVDD, DVSS	Buffered clock 13.56/6.78/3.39 MHz Output for external MCU
12	DVDD	Power	DVDD, DVSS	Digital and I/O VDD
13	DVSS	Power	DVDD, DVSS	Digital and I/O Ground
14	IRQ	OUT	DVDD, DVSS	Interrupt Request
15	MISO	OUT	DVDD, DVSS	SPI Master-In-Slave-Out
16	MOSI	IN	DVDD, DVSS	SPI Master-Out-Slave-In
17	SCLK	IN	DVDD, DVSS	SPI Clock Input
18	NCS	IN	DVDD, DVSS	SPI Chip Select (Active low)
19	RSTPD	IN	DVDD, DVSS	Reset and Power Down (Active High)
20	NC	-	-	Not Connected
21	NC	-	-	Not Connected
22	AVDD	PWR	AVDD, AVSS	Analog VDD (Optional)
23	TA	OUT	AVDD, AVSS	Analog Test Pin
24	NC	-	-	Not Connected
25	RX	IN	AVDD, AVSS	Receiver Input
26	VMID	IN	AVDD, AVSS	Mid Rail Reference Voltage
27	OSC1	IN	AVDD, AVSS	Xtal Oscillator input
28	OSC2	OUT	AVDD, AVSS	Xtal Oscillator Output
29	AVSS	Power	AVDD, AVSS	Analog Ground
30	AVDD	Power	AVDD, AVSS	Analog VDD
31	VREGA	Power	AVSS	3.3V Regulator Output for Analog part
32	VREGIN	Power	AVDD, AVSS	Regulator input

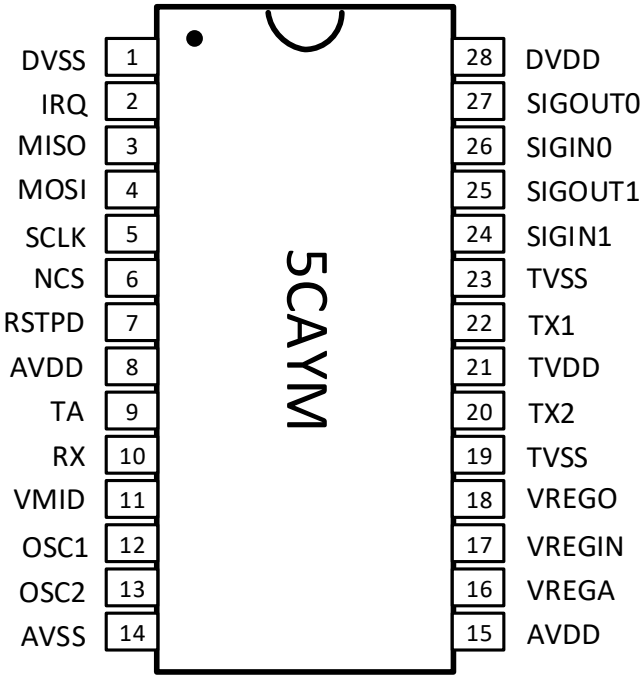


Figure 5 Pin arrangement (top view)

Y : Year Code
M : Month Code

Table 2 TSSOP Pin Description

Pin	Symbol	Type	Related SUPPLY	Description
1	**DVSS**	Power	DVDD, DVSS	Digital and I/O Ground
2	**IRQ**	OUT	DVDD, DVSS	Interrupt Request
3	**MISO**	OUT	DVDD, DVSS	SPI Master-In-Slave-Out
4	**MOSI**	IN	DVDD, DVSS	SPI Master-Out-Slave-In
5	**SCLK**	IN	DVDD, DVSS	SPI Clock Input
6	**NCS**	IN	DVDD, DVSS	SPI Chip Select (Active low)
7	**RSTPD**	IN	DVDD, DVSS	Reset and Power Down (Active High)
8	**AVDD**	PWR	AVDD, AVSS	Analog VDD (Optional)
9	**TA**	OUT	AVDD, AVSS	Analog Test Pin
10	**RX**	IN	AVDD, AVSS	Receiver Input
11	**VMID**	IN	AVDD, AVSS	Mid Rail Reference Voltage
12	**OSC1**	IN	AVDD, AVSS	Xtal Oscillator input
13	**OSC2**	OUT	AVDD, AVSS	Xtal Oscillator Output
14	**AVSS**	Power	AVDD, AVSS	Analog Ground
15	**AVDD**	Power	AVDD, AVSS	Analog VDD
16	**VREGA**	Power	AVSS	3.3V Regulator Output for Analog part
17	**VREGIN**	Power	AVDD, AVSS	Regulator input
18	**VREGO**	Power	DVDD, DVSS	3.3V Regulator Output for Digital part
19	**TVSS**	Power	TVDD, TVSS	Transmitter Ground
20	**TX2**	OUT	TVDD, TVSS	Transmitter Output 2
21	**TVDD**	Power	TVDD, TVSS	Transmitter VDD
22	**TX1**	OUT	TVDD, TVSS	Transmitter Output 1
23	**TVSS**	Power	TVDD, TVSS	Transmitter Ground
24	**SIGIN1**	IN	DVDD, DVSS	Digital input signal for test mode. If this Pin is unused, tide gnd.
25	**SIGOUT1**	OUT	DVDD, DVSS	Digital output signal for test mode
26	**SIGIN0**	IN	DVDD, DVSS	Digital input signal for test mode. If this Pin is unused, tide gnd.
27	**SIGOUT0**	OUT	DVDD, DVSS	Digital output signal for test mode
28	**DVDD**	Power	DVDD, DVSS	Digital and I/O VDD

Electrical specification

Table 3 Operating conditions

Parameter	Description	Min	Typ	Max	Unit	Conditions
AVDD	Analog Power Supply Voltage	2.7	3.3	3.6	V	
DVDD	Digital Power Supply Voltage	2.7	3.3	3.6	V	
TVDD	Transmitter Power Supply Voltage	2.7	5	7	V	
ESD	Electrostatic discharge tolerance	2			kV	HBM model
VPOR	Reset Trigger voltage		2.4		V	

Table 4 Power consumption

Parameter	Description	Min	Typ	Max	Unit	Conditions
IAVDD	Analog Power Supply Current		5.5		mA	All blocks active
			1.4		mA	Idle (Receiver Off)
			1.3		mA	Standby
			5.5	11.0	uA	Soft Power down
			0.5	1	uA	Hard Power down, (**RSTPD** = 1)
IDVDD	Digital Power Supply Current		2.5		mA	**CLKBF** is not enabled
			3.0		mA	**CLKBF** is enabled
			64		uA	Standby
			0.5	1	uA	Soft/Hard Power down

Table 5 Transmitter characteristic

Parameter	Description	Min	Typ	Max	Unit	Conditions
ITX1	Logic 1 Transmitter Source Current	175	200		mA	TVDD = 5V, 85 °C
		250	300		mA	TVDD = 7V, 85 °C
ITX0	Logic 0 Transmitter Sink Current	220	270		mA	TVDD = 5V, 85 °C
		330	350		mA	TVDD = 7V, 85 °C
ZTX	Tx Output impedance(GsCfgCW =0x3F)		7.5	9	Ohm	TVDD = 5V, 85 °C
			6.5	8	Ohm	TVDD = 7V, 85 °C
ITVDD	Transmitter Static Power supply Current		7		mA	**TX1** & **TX2** are Unconnected **RF1En** = 1, **RF2En** = 1 TVDD = 5 V
M	Adjustable Modulation index		-	100	%	TVDD = 5V

Table 6 Receiver characteristic

Parameter	Description	Min	Typ	Max	Unit	Conditions
VSEN	Receiver input sensitivity		1		mVpkpk	AVDD = 3.3V
PSRR	Power supply rejection ratio		40		dB	AVDD = 3.3V + 0.2*sin(1MHz)
VRx	Rx input voltage range	0.0		3.3	V	AVDD = 3.3 Volt, **BypassENV** = 0
		0.5		2.8	V	AVDD = 3.3 Volt, **BypassENV** = 1
VCarMin	Minimum Carrier for envelope detector		0.3		Vpkpk	
VVMID	VMID Voltage		1.65		V	**VMidsel** = 0, AVDD = 3.3 V
			1.24		V	**VMidsel** = 1, AVDD = 3.3 V
ZVMID	VMID output impedance @ 13.56 MHz		6		ohm	CLoad(1) = 100nF, TVDD = 5 V
Gain	Gain (Measured from Rx to the output of the internal last amplifier)			48	dB	**Gain**= 11b, **Gain_ST3** = 000b
		12			dB	**Gain** = 00b, **Gain_ST3** = 000b
Gstep	Gain step		3		dB	**AGCEN** = 1
			12		dB	**AGCEN** = 0 Defined by **Gain[1:0]**
RxNoise	Intrinsic input referred noise in Rx		TBD		mVrms	

(1) CLoad : Load capacitance at **VMID** pin

Table 7 Regulator characteristics

Parameter	Description	Min	Typ	Max	Unit	Conditions
VREGIN	Regulator input voltage	4.5	5	7	V	
VREGOUT	Regulator output voltage	3.10	3.25	3.4	V	IREGOUT = 0 mA
IREGIN	Input regulator current			160	mA	
IREGOUT	Output regulator current			80	mA	
$\Delta Vout_{LineReg}$	Line regulation (ΔVout)		0.5	1	mV/V	IREGOUT = 0 mA , 4.5V < **VREGIN** < 7V
$\Delta Vout_{LoadReg}$	Load regulation (ΔVout)		0.25		mV/mA	**VREGIN** = 5 V , 0 < IREGOUT < 80 mA
VREGDrop	Drop Out Voltage			40	mV	IREGOUT = 80 mA
IREGBias	Regulator Bias Current	170	200	220	uA	5 V < **VREGIN** < 7 V